REMARKS

Claims 1-11 and 14-17 are pending in the present application. In the Office Action mailed November 28, 2007, Claims 1-10 and 14-17 are rejected under 35 U.S.C. § 102(b) as being anticipated by Johnson, U.S. Patent No. 5,898,701. Claim 11 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Johnson in view of Lindholm, U.S. Patent No. 6,553,523.

Applicant gratefully acknowledges the telephone conference with the Examiner and John King, a representative for the Applicant, on February 7, 2008 during which proposed amendments were discussed. As discussed during the telephone conference, Applicant believes that the claims as amended clearly distinguish over the cited references.

In response to the rejection of the claims, Applicant has amended each of the independent claims to more clearly indicate that the device has both programmable logic and a JTAG interface, and that configuration process signals are provided to an input/output pin which is separate from the JTAG interface. In particular, Applicant has amended independent Claim 1 to include a step of "providing a connection between a configuration device and an input/output pin of the device having programmable logic which is separate from the JTAG interface." Applicant has further amended the step of verifying the connection to indicate that it is verifying a connection between the configuration device and the device having programmable logic. Finally, Applicant has further amended Claim 1, as well as dependent Claims 2-6, in view of the amendment to the preamble of Claim 1.

Applicant has similarly amended Claim 9 to indicate that the system comprises a device having programmable logic and a JTAG interface, and that the device is coupled to receive a configuration bitstream by way of an input/output (I/O) pin which is separate from the JTAG interface. Applicant has also amended claim 1 to indicate that the configuration device is coupled to the I/O pin of the device having programmable logic. Applicant has also amended dependent Claim 11 in view of the amendment to Claim 9.

Applicant has also amended Claim 16 to indicate that the computer program has code sections for debugging a configuration process of a device having

programmable logic and a JTAG interface. Applicant has further amended Claim 16 to indicate that the step of coupling configuration process signals comprises coupling configuration process signals to an input/output pin of the device having programmable logic, where the input/output pin is separate from the JTAG interface.

Finally, Applicant has amended Claim 17 to indicate that the configuration analyzer is for debugging a device having programmable logic and a JTAG interface. Applicant has further amended the means for reconfiguring process signals to indicate that the configuration process signals are received by way of an input/output pin of the device having programmable logic separate from the JTAG interface.

Support for the above described amendments to each of the claims may be found at least in Figs. 3 and 4, paragraph [0031], lines 5-19, and paragraph [0032], lines 1-9.

Applicant respectfully submits that the claims as amended clearly distinguish over Johnson. As set forth in Applicant's claims, configuration data is provided to a device having an input/output pin separate from the JTAG interface. Before specifically addressing the amendments presented in this response, Applicant again notes that Johnson not only fails to disclose or even suggest a configuration bitstream, but also that the boundary scan register of Johnson is merely shown for purposes of completeness and is not required in order to practice the invention. (Col.5, lines 29-33). Further, the JTAG chain of Johnson relates to data input to the JTAG interface, and not an input/output pin separate from the JTAG interface as claimed. There is simply no teaching or even a suggestion in Johnson that a boundary scan register of Johnson is coupled to an input/output pin receiving configuration process signals. In contrast, Johnson merely teaches that a boundary scan register is coupled to either a test data input (TDI) signal, a test clock (TCK) or decoded test mode select (TMS) signal. That is, each figure of Johnson discloses the transfer of data by way of the TDI signal. There is also no teaching or suggestion that the circuit of Johnson enables verifying a connection to an input/output pin of the programmable logic device coupled to receive the configuration process signals. Applicant respectfully submits that each of the independent Claims 1, 9, 16 and 17 as amended clearly distinguish over Johnson, and respectfully request reconsideration of the rejection. Applicant also

submits that dependent Claims 2-8, 10-11, and 14-15 are allowable for at least the same reasons that the independent claims are believed allowable.

In response to the rejection of Claim 11, Applicant respectfully submits that Claim 11 is allowable over the combination of references for the same reasons that Claim 9 is believed allowable over Johnson alone. That is, Lindholm is cited for disclosing a field programmable gate array. However, Lindholm also fails to disclose or suggest a configuration analyzer analyzing configuration process signals stored in boundary scan registers of the programmable logic device during the configuration process, as claimed in independent Claim 9. Applicant respectfully requests reconsideration of Claim 11.

CONCLUSION

Applicant believes that Claims 1-11 and 14-17 are in condition for allowance, and allowance of the application is therefore requested. If action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicant's attorney, Justin Liu, at 408-879-4641.

Respectfully submitted,

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I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent & Trademark Office on February 28, 2008.
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